

ENSSAT
2^{ème} Année EII

16/06/09
Durée 2H

Devoir d'interfaçage
Carte d'interface par FIFO.

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façage
par FIFO.

ENSSAT
2^{ème} Année EII

Devoir d'inter
Carte d'interface

Documents autorisés : cours, TD, TP

Principe et composants :

eur AT91M55800 à 16 Mhz (fréquence

Le système concevoir vise à interfacé 2 cartes processeur AT91M55800 à 16 Mhz (fréquence effective après PLL) via 2 mémoires de type FIFO.

ement des données en
rsque la FIFO est
l suffit de lire
es à l'autre processeur
onnées vers l'entrée de
t évidemment
é pour afficher une partie des données des FIFO.
de données, il s'agit de connecter le _W de la
la réception de données, il s'agit de connecter le

L'utilisation de mémoires FIFO à double accès permet de stocker facilement les envoyant séquentiellement sur les entrées de la FIFO. Une ligne indique la FIFO pleine, une ligne à moitié pleine et une ligne vide. Pour récupérer les données, on lit séquentiellement les sorties de la FIFO. Chaque processeur transmet des données via une FIFO de type Am7202A de 1024 x 9. Chaque processeur envoie des données à la FIFO et récupère des données de la FIFO.

e sortie autorisant l'écriture d'octets, la seconde
la lecture d'octets. Le 9^{ème} bit n'est pas utilisé.
s de signalisation des 2 FIFOS :
FIFO à moitié remplie (half full).
s lignes différentes du bus de données D0, D1,

caractères sont codés en ASCII. L'afficheur sera utilisé pour afficher les données. La première FIFO Am7202A est utilisée pour l'envoi des données. La deuxième FIFO Am7202A est utilisée pour la réception des données. Les signaux de commande sont : _R, _W, _EF, _FF, _HF. Elles auront la même adresse mais seront gérées sur des lignes différentes du bus de données D0, D1, D2 pour la première, D4, D5, D6 pour la seconde.

signaux classiques du bus AT91M55800 en

Les signaux d'adresses et de contrôle du bus sont les suivants : _A0, _A1, _A2, _A3, _A4, _A5, _A6, _A7, _A8, _A9, _A10, _A11, _A12, _A13, _A14, _A15, _A16, _A17, _A18, _A19, _A20, _A21, _A22, _A23, _A24, _A25, _A26, _A27, _A28, _A29, _A30, _A31, _A32, _A33, _A34, _A35, _A36, _A37, _A38, _A39, _A40, _A41, _A42, _A43, _A44, _A45, _A46, _A47, _A48, _A49, _A50, _A51, _A52, _A53, _A54, _A55, _A56, _A57, _A58, _A59, _A60, _A61, _A62, _A63, _A64, _A65, _A66, _A67, _A68, _A69, _A70, _A71, _A72, _A73, _A74, _A75, _A76, _A77, _A78, _A79, _A80, _A81, _A82, _A83, _A84, _A85, _A86, _A87, _A88, _A89, _A90, _A91, _A92, _A93, _A94, _A95, _A96, _A97, _A98, _A99, _A100, _A101, _A102, _A103, _A104, _A105, _A106, _A107, _A108, _A109, _A110, _A111, _A112, _A113, _A114, _A115, _A116, _A117, _A118, _A119, _A120, _A121, _A122, _A123, _A124, _A125, _A126, _A127, _A128, _A129, _A130, _A131, _A132, _A133, _A134, _A135, _A136, _A137, _A138, _A139, _A140, _A141, _A142, _A143, _A144, _A145, _A146, _A147, _A148, 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_A1756, _A1757, _A1758, _A1759, _A1760, _A1761, _A176

Les chronogrammes et les timings de la FIFO et de l'afficheur sont fournis. Les adresses disponibles sont situées à partir de B8000000 H. Un seul chip select _CSR5 du processeur activera l'application. Le complément de décodage est réalisé à partir des autres signaux du processeur.

Conception matérielle

- 1) Faire une proposition d'adresses pour chaque circuit en utilisant au maximum 1 Koctet d'adressage pour l'ensemble de l'application en justifiant vos réponses. Ecrire les équations de sélection des circuits en incluant les signaux de lecture et d'écriture si nécessaire, utiliser un ou plusieurs circuits de type PAL 16L8. Préciser les signaux nécessaires au décodage.
- 2) Etablir un schéma de câblage faisant apparaître les composants, les bus, les signaux de contrôle, le ou les circuits PAL de décodage. Pour plus de clarté plutôt qu'un schéma global représenter de préférence les connexions élément par élément. Pour le décodage par PAL préciser l'affectation des broches.

Pour les questions suivantes on considère un délai de traversée du circuit PAL égal à 5ns.

- 3) Déterminer en examinant précisément les timings en lecture et écriture des FIFO Am7202A si le timing est compatible avec celui du bus. On ne prendra pas en compte les signaux de synchronisation gérés par le LS 244. En fonction des timings possibles de la FIFO en choisir une parmi celles proposées. Si problème proposer des solutions pour assurer la compatibilité.
- 4) Préciser la programmation complète du registre de contrôle EBI_CSR5 en ne prenant en compte que les FIFO.
- 5) Que pensez-vous en première analyse (temps de cycle, largeur d'impulsion, des chronogrammes en écriture de l'afficheur LCD, DMC24227, relativement au processeur à 16 Mhz. Quel type de solution peut-on envisager pour adapter le temps de maintien tDHW ?

Conception logicielle (langage C)

La gestion des FIFO est réalisée par scrutation par scrutation du LS244.

Déclarer les variables utilisées pour l'affichage

- 1) Ecrire une fonction d'envoi de 2048 échantillons vers la FIFO, les échantillons sont envoyés à partir d'un tableau déclaré en variable globale. L'envoi s'effectue dès que la FIFO est à moitié vide (indicateur à moitié pleine) jusqu'à FIFO pleine.
- 2) Ecrire la fonction de lecture dans un tableau de 2048 échantillons. Lecture dès que FIFO non vide. Lorsque le tableau est plein sauvegarder les 16 premiers éléments, puis remplacer les premiers éléments chargés par les nouveaux échantillons reçus.
- 3) Ecrire une fonction qui convertit un octet sous forme hexadécimale ASCII pour affichage (ex 140 : "8C ") ; on pourra utiliser un tableau de conversion qui à partir de l'indice va fournir le code ASCII.

Char CONV[16]={ '0','1','2','3','4','5','6','7','8','9','A','B','C','D','E','F' } ;

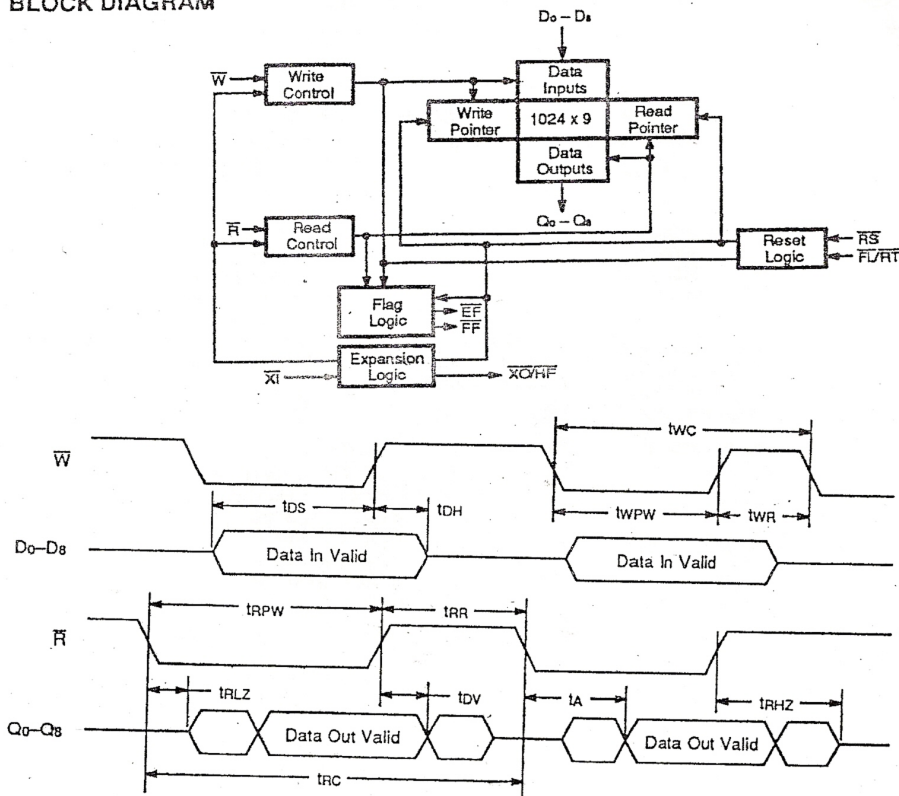
- 4) Ecrire une fonction pour afficher lors de la lecture de la FIFO d'entrée les 16 premiers octets lus sur le LCD (séparés par le caractère « espace » ' '). Les 8 premiers octets sur la ligne 0, les 8 suivants sur la ligne 1. L'affichage sur le LCD se fait en ASCII. Pour chaque accès à l'afficheur, attendre afficheur prêt (bit 7 du registre d'état=0). Sélectionner la ligne 0 de l'afficheur en envoyant le code 0x80 dans le registre de contrôle, (pour la ligne 1 code 0xC0) ; puis envoyer successivement chaque caractère à afficher dans le registre de données (type auto-incrémenté).

Documentation : LCD, FIFO

Am7202A

High Density First-In First-Out (FIFO)
1024 x 9-Bit CMOS Memory

BLOCK DIAGRAM



15491B-6

Asynchronous Write and Read Timing

SWITCHING CHARACTERISTICS over COMMERCIAL operating range unless otherwise specified

Parameter Symbol	Parameter Description	Figures	Am7202A-15		Am7202A-25		Am7202A-35		Am7202A-50		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Write and Flag Timing											
t _{WC}	Write Cycle Time	3	25		35		45		65		ns
t _{WPW}	Write Pulse Width	3	15		25		35		50		ns
t _{WR}	Write Recovery Time	3	10		10		10		15		ns
t _{DS}	Data Setup Time	3,9	12		15		18		30		ns
t _{DH}	Data Hold Time	3,9	0		0		0		5		ns
t _{WFF}	Write LOW to Full Flag LOW	6,9		24		25		30		45	ns
t _{WHF}	Write LOW to Half-Full Flag LOW	5		30		35		45		65	ns
t _{WEF}	Write HIGH to Empty Flag HIGH	4,8		24		25		30		45	ns
t _{WLZ}	Write Pulse HIGH to Data Bus at LOW Z (Note 1)	8	5		5		10		10		ns
t _{WPF}	Write Pulse Width after FF HIGH	9	15		25		35		50		ns
Read and Flag Timing											
t _{RC}	Read Cycle Time	3	25		35		45		65		ns
t _A	Access Time	3,4,8,9		15		25		35		50	ns
t _{RR}	Read Recovery Time	3	10		10		10		15		ns
t _{RPW}	Read Pulse Width	3	15		25		35		50		ns
t _{RLZ}	Read Pulse LOW to Data Bus at LOW Z (Note 1)	3	5		5		5		5		ns
t _{DV}	Data Valid from Read Pulse HIGH	3	5		5		5		5		ns
t _{RHZ}	Read Pulse HIGH to Data Bus at HIGH Z (Note 1)	3		15		18		20		30	ns
t _{RFF}	Read HIGH to Full Flag HIGH	6,9		24		25		30		45	ns
t _{RHF}	Read HIGH to Half-Full Flag HIGH	5		30		35		45		65	ns
t _{REF}	Read LOW to Empty Flag LOW	4,8		24		25		30		45	ns
t _{RPE}	Read Pulse Width after EF HIGH	8	15		25		35		50		ns

AM7202A (2)

Pas d'utilisation des modes "Expansion"



PIN DESCRIPTION

D0-8

Data In (Inputs (9))

These nine pins are the data inputs to the FIFO.

EF

Empty Flag (Output; Active LOW)

The HIGH state of the Empty Flag (EF) indicates that the FIFO contains data to be read. The EF goes LOW when the read pointer is equal to the write pointer, indicating that the device is empty. EF LOW inhibits further Read operations.

The EF goes HIGH after the rising edge of Write (W) during the first write cycle for an empty FIFO (See Figure 4). The EF goes LOW after the falling edge of Read (R) during the read cycle which creates the empty condition.

During a Reset cycle, the EF is driven LOW (active).

FF

Full Flag (Output; Active LOW)

The HIGH state of the Full Flag (FF) indicates that the FIFO is capable of accepting data. The FF goes LOW when the write pointer is one location less than the read pointer, indicating that the device is full. FF LOW inhibits further Write operations.

The FF goes HIGH after the rising edge of Read (R) during the first read cycle following a full condition (See Figure 6). The FF goes LOW after the falling edge of Write (W) during the write cycle which creates the full condition.

During a Reset cycle, the FF is driven HIGH (inactive).

FL/RT

First Load/Retransmit (Input; Active LOW)

This is a dual purpose input, dependent upon whether the FIFO is in Single Device Mode or Depth-Expansion Mode.

This pin acts as a FIRST LOAD (FL) pin when in the Depth-Expansion Mode. The device receiving data first will have the FL input tied LOW, while the remaining devices will have the FL pin tied HIGH. The states of the FL and Expansion In (XI) pins are used to determine the FIFO's mode of operation, as shown in Tables 1 and 2.

This pin is used as the Retransmit (RT) input during Single Device Mode. The device can be instructed to retransmit the previously written data when RT is pulsed LOW.

GND

Power Supply, Ground

This pin is the 0 V power supply for the FIFO.

NC

No Connect

These pins are not connected.

Q0-8

Data Out (Outputs (9), Three State)

These nine pins are the data outputs for the FIFO. These pins are in a high impedance state whenever Read (R) is HIGH.

R

Read (Input; Active LOW)

The falling edge of Read (R) initiates a read cycle, except when the device is empty, as indicated by the Empty Flag (EF) being LOW. Valid data appears on the outputs (Q0-8) after the falling edge of R. After R goes HIGH, the Data Outputs (Q0-8) will return to a high impedance condition.

RS

Reset (Input; Active LOW)

The falling edge of Reset (RS) is used to reset the FIFO. During Reset, both the read and write pointers are set to the first location in the FIFO. Since the reset cycle initializes the FIFO to an empty condition, the Empty Flag (EF) is driven LOW (active), and both the Half-Full Flag (HF) and Full Flag (FF) are driven HIGH (inactive).

Vcc

Power Supply

This pin is the +5 V power supply for the FIFO.

W

Write (Input; Active LOW)

The falling edge of Write (W) initiates a write cycle, except when the device is full, as indicated by the Full Flag (FF) being LOW. Data is latched into the FIFO on the rising edge of W.

XI

Expansion In (Input; Active LOW)

Expansion In (XI) is grounded to indicate operation in the Single Device or Width-Expansion Modes. In Depth Expansion Mode, the XI pin is connected to the Expansion Out (XO) pin of the previous device, except for the XI pin of the first device which is connected to the XO pin of the last FIFO.

This pin operates at CMOS logic levels, thus providing noise immunity between cascaded devices.

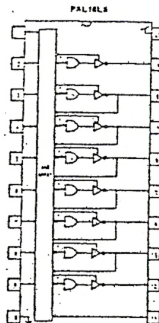
XO/HF

Expansion Out/Half-Full Flag (Output; Active LOW)

This is a dual purpose output, dependent upon whether the device is in Single Device Mode or Depth Expansion Mode.

This pin operates as an Expansion Out (XO) signal during Depth Expansion Mode. In this mode, the XO pin is connected to the Expansion Input (XI) pin of the following device, except for the XO pin of the last device which is connected to the XI pin of the first device.

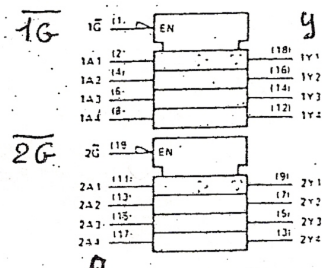
20-Pin Medium PAL Family



PAL 16 L8

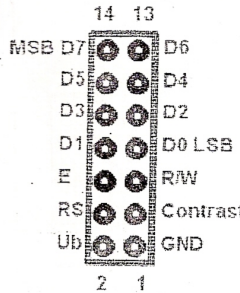
10 entrées
2 sorties
6 entrées ou sorties

logic symbol



LS 244

Table 1: Character LCD Pinout

		Pin#	Name		In/Out/Pwr
	1	GND	Ground		Power
	2	VCC	LCD Controller Power (+3 to +5V)		Power
	3	VLCD	LCD Display Bias (+5 to -5V *see text)		Analog
	4	RS	Register Select: H: Data L: Command		Input
	5	R/W	H: Read L: Write		Input
	6	E	Enable (Data strobe, active high)		Input
	7	DB0	Data LSB		I/O
	8	DB1	Data		I/O
	9	DB2	Data		I/O
	10	DB3	Data		I/O
	11	DB4	Data		I/O
	12	DB5	Data		I/O
	13	DB6	Data		I/O
	14	DB7	Data MSB		I/O
	15	A	LED Backlight Anode (optional)		Power
	16	K	LED Backlight Cathode (optional)		Power

Pins 4,5, and 6 are the control lines for the LCD. These lines indicate what kind of transaction you are proposing to do over the data lines DB0-7. The state of RS indicates whether you wish to transfer commands or display data. The R/W line indicates whether you intend to read or write. Finally, the E line tells the display when you are actually ready to perform the transaction. The control lines RS, R/W, and E, along with the data lines DB0-7 are standard digital logic inputs or outputs. Remember than when performing reads you must set the port connected to DB0-7 to be input.

3. Accessing your LCD module

Character LCD modules are accessed through only two "registers", the Command Register, and the Data Register. When you perform a read or write with RS low, you are accessing the Command Register and giving the module instructions. When you read or write with RS high, you are accessing the Data Register and reading or writing characters/data from or to the display.

2.3.AC Characteristics

$V_{CC}=5.0V\pm10\%$

Parameter	Symbol	Conditions	Min.	Max.	Units
Enable Cycle Time	t_{CYC}	Fig.1, 2	500	—	ns
Enable Pulse Width	P_{WEH}	Fig.1, 2	230	—	ns
Enable Rise/Fall Time	t_{ER}, t_{EF}	Fig.1, 2	—	20	ns
Address Setup Time	t_{AS}	Fig.1, 2	40	—	ns
Address Hold Time	t_{AH}	Fig.1, 2	10	—	ns
Write Data Setup Time	t_{DSW}	Fig.1	80	—	ns
Write Data Hold Time	t_{DHW}	Fig.1	10	—	ns
Read Data Delay Time	t_{DDR}	Fig.2	—	160	ns
Read Data Hold Time	t_{DHR}	Fig.2	5	—	ns

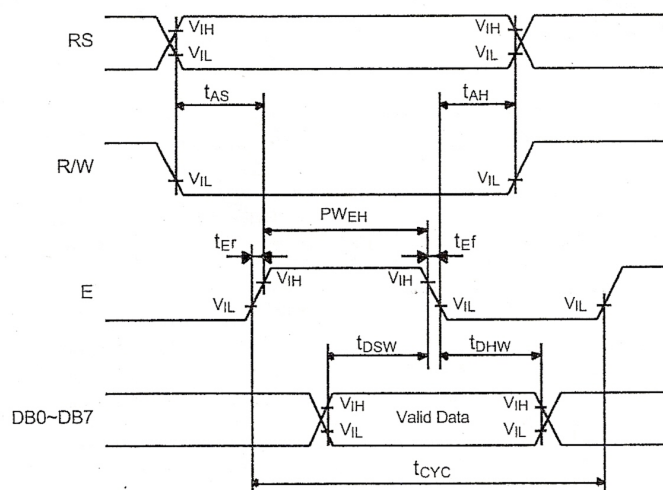


Fig.1 Write Operation Timing

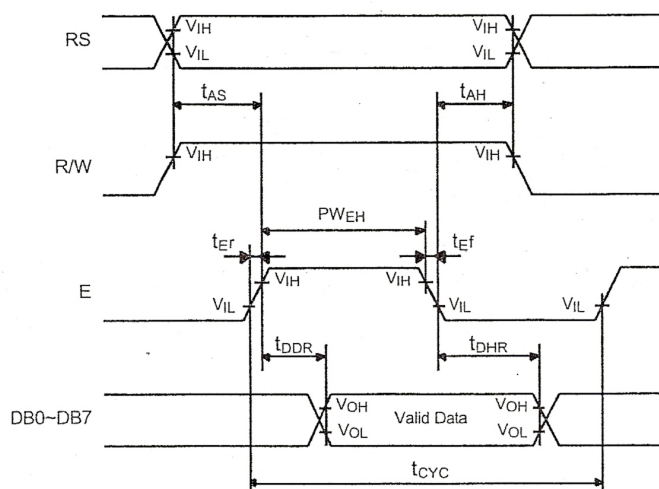


Fig.2 Read Operation Timing